



HTN036N03P DFN5x6 TN036N03P

Absolute Maximum Ratings at $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Parameter	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$T_c=25^{\circ}\text{C}$	70	A
	$T_c=100^{\circ}\text{C}$	64	A
Drain to Source Voltage	V_{DS} -	30	V
		± 20	V
Pulsed Drain Current		70	A
		54	mJ
		50	W
		-55 to 150	$^{\circ}\text{C}$

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	R_{JC}	2.5	$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction-Ambient	R_{JA}	50	$^{\circ}\text{C}/\text{W}$



Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=24V, T_j=25^{\circ}C$	-		
	$R_{DS(on)}$		-	3 4.2	3.6
Transconductance	g_{fs}		-	25.2	- S
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}$ Open, $f=1MHz$	-	2.0	-

Dynamic Characteristics

Input Capacitance	C_{iss}		-	2015	
		$V_{GS}=0V, V_{DS}=15V, f=1MHz$	-	365	- pF
Reverse Transfer Capacitance	C_{rss}		-	205	-
Total Gate Charge (10V)	Q_g (10V)		-	42	-
	Q_g (4.5V)	$V_{DD}=15V, I_D=18A, V_{GS}=10V$	-	21	- nC
	Q_{gs}		-	6	-
	Q_{gd}		-	9	-
Turn on Delay Time	$t_{d(on)}$		-	15	-
Rise time	t_r	$V_{DD}=15V, I_D=1A, V_{GS}=10V, R_G=6 \Omega$	-	20	- ns
Turn off Delay Time	$t_{d(off)}$		-	72	-
Fall Time	t_f		-	20	-

Reverse Diode Characteristics

Reverse Recovery Charge	Q_{rr}	$V_{GS}=0V, I_F=15A$	-	0.7	1.1
			-	15.0	- ns
		$I_F=15A, di_F/dt=100A/\mu s$	-	8.0	- nC

Figure 1. Typical Output Characteristics

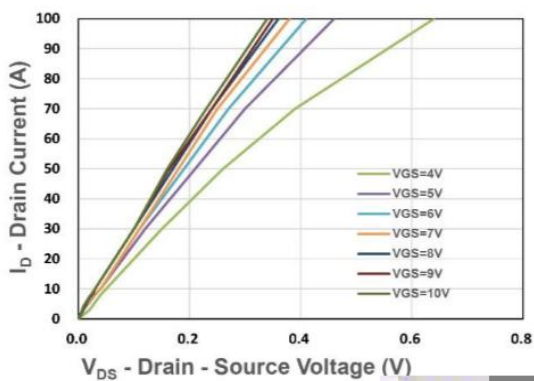


Figure 2. On-Resistance vs. Gate-Source Voltage

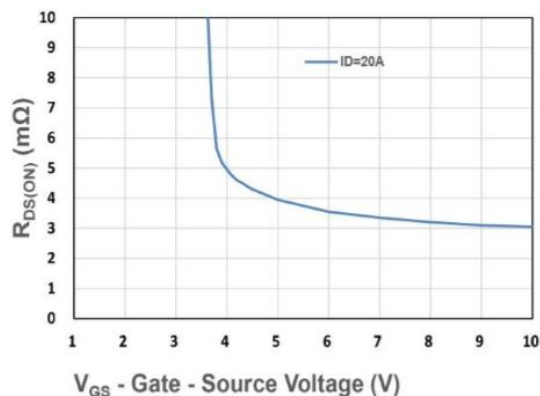


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

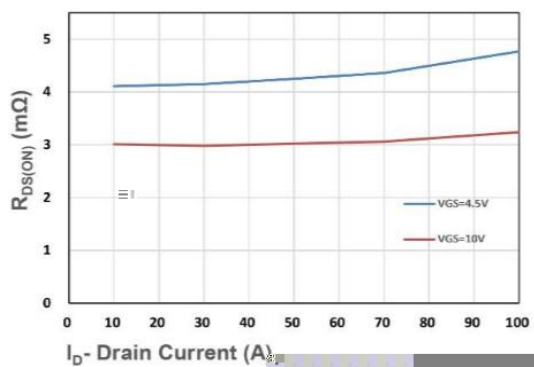


Figure 4. Normalized On-Resistance vs. Junction Temperature

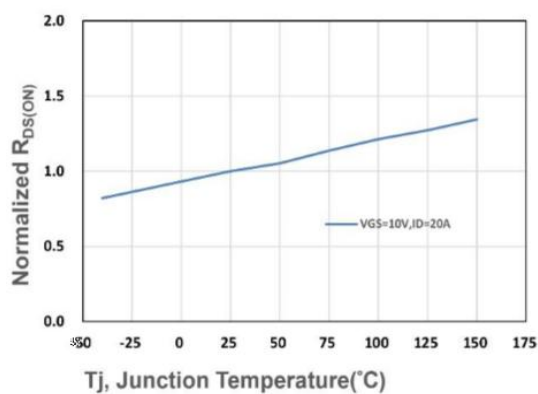


Figure 5. Normalized Threshold Voltage VS Junction Temperature

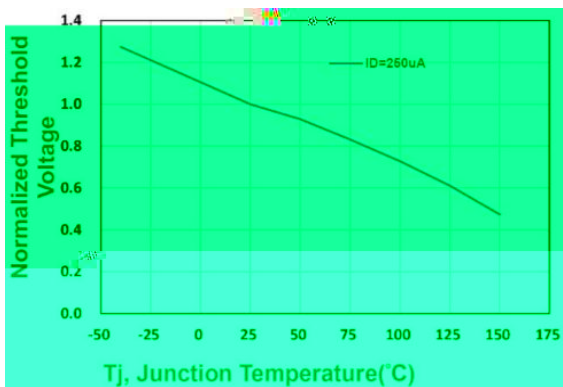


Figure 6. Typical Source-Drain Diode Forward Voltage

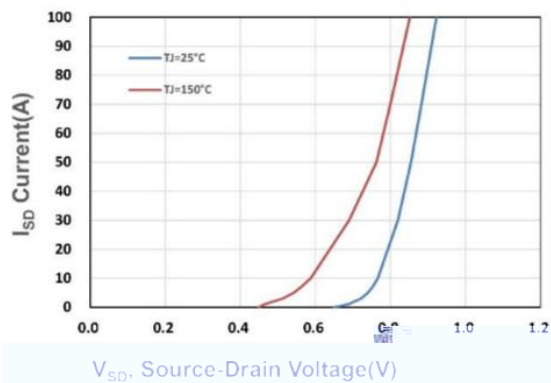


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

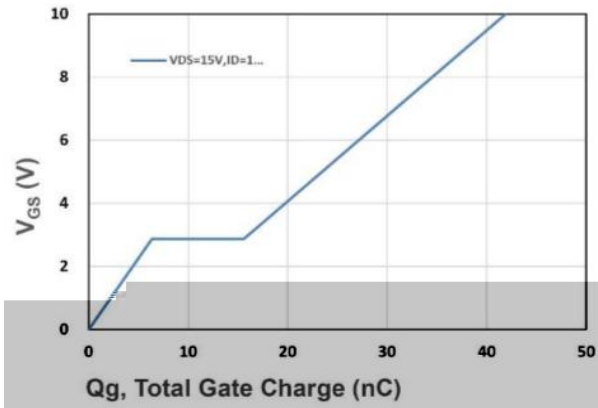


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

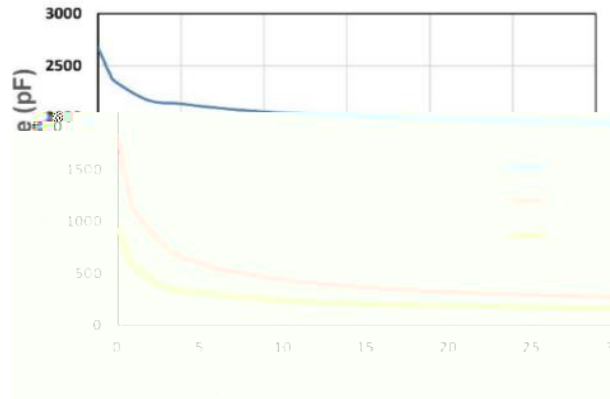


Figure 9. Maximum Safe Operating Area

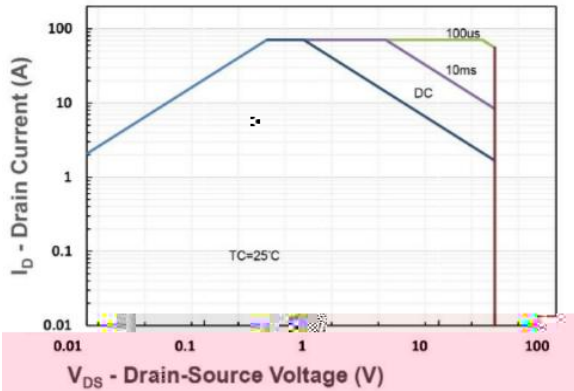


Figure 10. Maximum Drain Current vs. Case Temperature

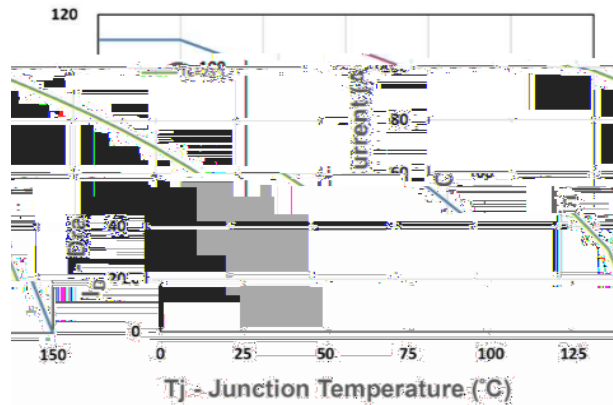
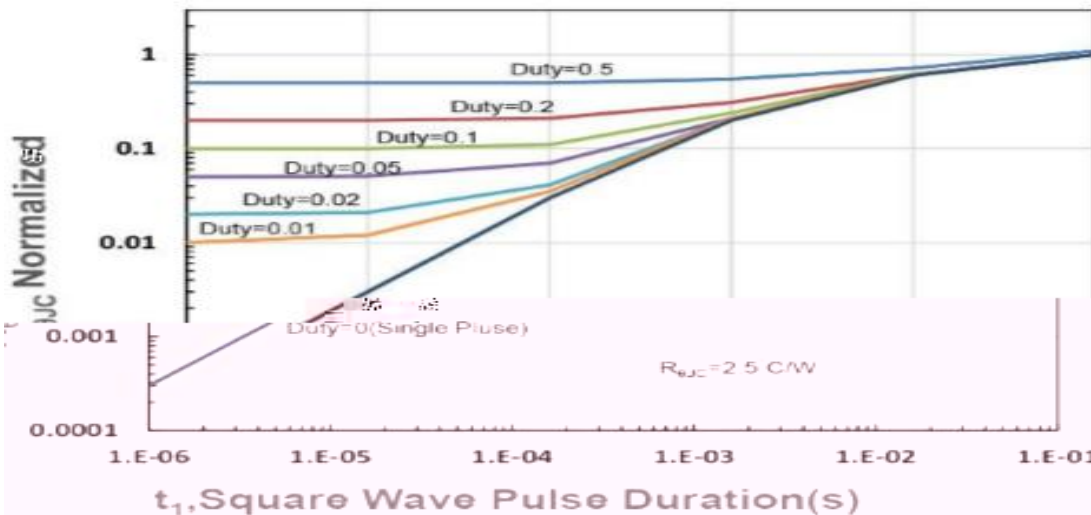
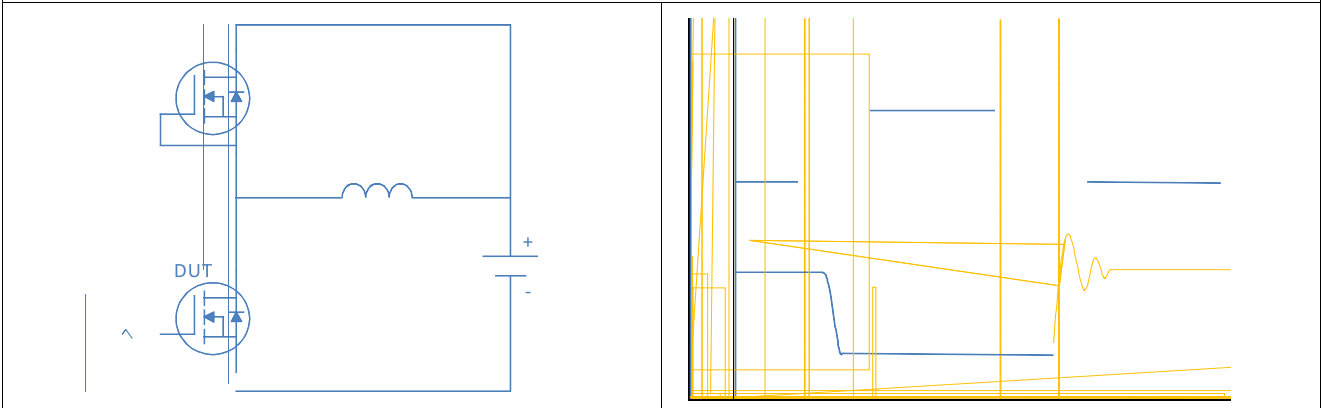


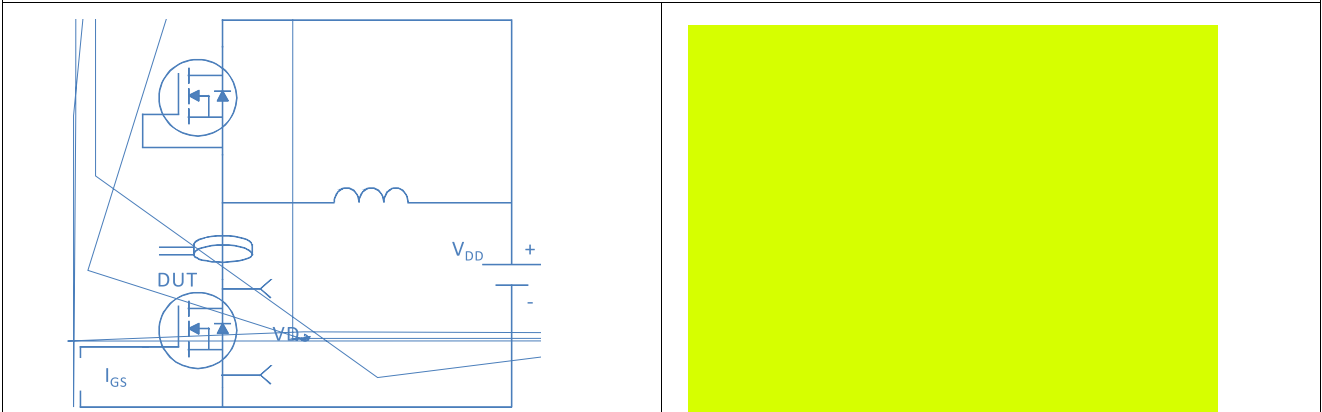
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



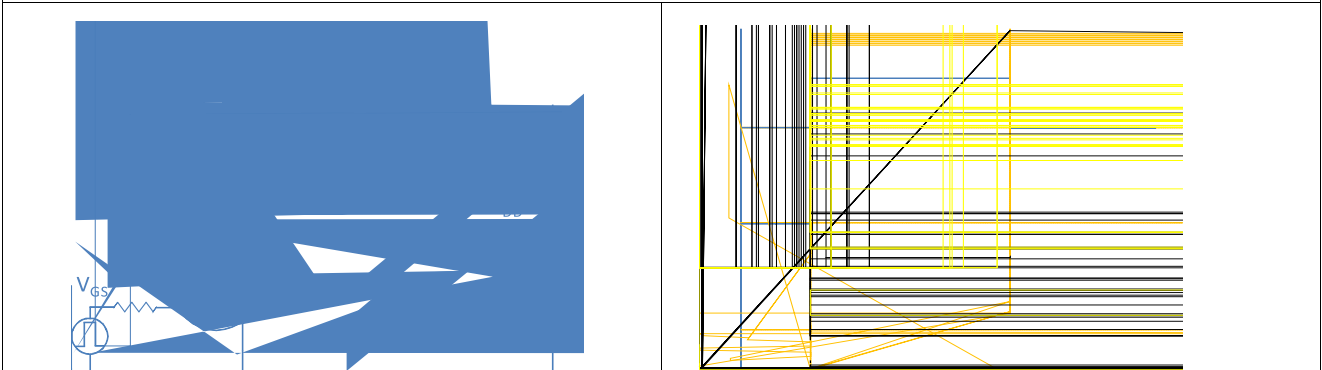
Inductive switching Test



Gate Charge Test



Uclamped Inductive Switching (UIS) Test



Diode Recovery Test

